



**IDG-21X0 & IXZ-21X0 Product  
Specification**

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Revision: 1.2  
Release Date: 05/24/2011

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Product Specification  
Revision 1.2**

Preliminary



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### 1 Document Information

#### 1.1 Revision History

Revision Date	Revision	Description
04/11/2011	1.0	Initial Release
04/14/2011	1.1	Improved Electrical Specifications (Section 3.1)
05/24/2011	1.2	Sec. 1.4 Added section describing InvenSense software solutions Sec. 4.1 Specified CLKIN to be connected to GND if unused Sec. 4.4 Modified $T_{VDDR}$ value for consistency with Electrical Characteristics Sec. 4.4 Clarified $T_{VLG-VDD}$ value Sec. 7.4.3 Clarified Trace Routing precautions Sec. 7.5 Modified Package Marking diagrams for clarity



## 1.2 Purpose and Scope

This document is a product specification, providing a description, specifications, and design related information for the IDG-2100™, IDG-2150™, IXZ-2100™, and IXZ-2150™. The IDG-2100 and IDG-2150 together are called the IDG-21X0™, while the IXZ-2100, and IXZ-2150 together are called the IXZ-21X0™. These parts are dual axis parts where the IDG-21X0 contains X- and Y- axis gyros, while the IXZ-21X0 contains X- and Z- axis gyros. The IDG-21X0 and IXZ-21X0 are collectively referred to as IDG/IXZ-21X0™.

Electrical characteristics are based upon simulation results and limited characterization data of advanced samples only. Specifications are subject to change without notice. Final specifications will be updated based upon characterization of final silicon.

## 1.3 Product Overview

The IDG-21X0 and IXZ-21X0 are single-chip, digital-output, 2-axis MEMS gyro ICs with programmable full-scale ranges of  $\pm 250$ ,  $\pm 500$ ,  $\pm 1000$ , and  $\pm 2000$  degrees/sec (dps), which is useful for precision tracking of both fast and slow motions. Factory-calibrated initial sensitivity reduces production-line calibration requirements. The part's on-chip FIFO simplifies system timing and lower system power consumption. The FIFO allows a system microcontroller to burst read the sensor data and then go to sleep while the IDG/IXZ-21X0 collects more data.

Other industry-leading features include on-chip 16-bit ADCs, programmable digital filters, a precision clock with 1% variation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ , an embedded temperature sensor, and programmable interrupts. Parts are available with Fast-Mode I<sup>2</sup>C or SPI (IDG/IXZ-2100 only) serial interfaces, a VDD operating range of 2.1 to 3.6V, and a VLOGIC interface voltage from 1.71V to 3.6V (IDG/IXZ-2150 only).

By leveraging its patented and volume-proven Nasiri-Fabrication platform, which integrates MEMS wafers with companion CMOS electronics through wafer-level bonding, InvenSense has driven the IDG-21X0 and IXZ-21X0 package size down to a footprint of 4x4x0.9mm (QFN), while providing the highest performance, lowest noise, and the lowest cost semiconductor packaging to address a wide range of handheld consumer electronic devices. The device provides the highest robustness by supporting 10,000g shock in operation. The highest cross-axis isolation is achieved by design from its single silicon integration.

The IDG/IXZ-2100 and IDG/IXZ-2150 are identical, except that the IDG/IXZ-2150 supports the I<sup>2</sup>C serial interface only, and has a separate VLOGIC reference pin (in addition to its analog supply pin, VDD), which sets the logic levels of its I<sup>2</sup>C interface. The VLOGIC voltage may be between 1.71V min to VDD max. The IDG/IXZ-2100 supports both I<sup>2</sup>C and SPI interfaces and has a single supply pin, VDD, which is the device's logic reference supply and the analog supply for the part. The table below outlines these differences:

### Primary Differences between IDG/IXZ-2100 and IDG/IXZ-2150

Part / Item	IDG/IXZ-2100	IDG/IXZ-2150
VDD	2.1V to 3.6V	2.1V to 3.6V
VLOGIC	N/A	1.71V to VDD
Serial Interfaces Supported	I <sup>2</sup> C, SPI	I <sup>2</sup> C
Pin 8	/CS	VLOGIC
Pin 9	AD0/SDO	AD0
Pin 23	SCL/SCLK	SCL
Pin 24	SDA/SDI	SDA



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### 1.4 Software Solutions

This section describes the MotionApps™ software solutions included with the InvenSense MPU™ (MotionProcessing Unit™) and IMU (Inertial Measurement Unit) product families. Please note that the products within the IDG, IXZ, and ITG families do not include these software solutions.

The MotionApps Platform is a complete software solution that in combination with the InvenSense IMU and MPU MotionProcessor™ families delivers robust, well-calibrated 6-axis and/or 9-axis sensor fusion data using its field proven and proprietary MotionFusion™ engine. Solution packages are available for smartphones and tablets as well as for embedded microcontroller-based devices.

The MotionApps Platform provides a turn-key solution for developers and accelerates time-to-market. It consists of complex 6/9-axis sensor fusion algorithms, robust multi-sensor calibration, a proven software architecture for Android and other leading operating systems, and a flexible power management scheme.

The MotionApps Platform is integrated within the middleware of the target OS (the sensor framework), and also provides a kernel device driver to interface with the physical device. This directly benefits application developers by providing a cohesive set of APIs and a well-defined sensor data path in the user-space.

The table below describes the MotionApps software solutions included with the InvenSense MPU and IMU product families.

#### InvenSense MotionProcessor Devices and Included MotionApps Software

Feature	Included Software				Notes
	MotionApps	Embedded MotionApps	MotionApps Lite	Embedded MotionApps Lite	
Part Number	MPU-3050 MPU-6050		IMU-3000		
Processor Type	Mobile Application Processor	8/16/32-bit Microcontroller	Mobile Application Processor	8/16/32-bit Microcontroller	
Applications	Smartphones, tablets	TV remotes, health/fitness, toys, other embedded	Smartphones, tablets	TV remotes, health/fitness, toys, other embedded	
6-Axis MotionFusion	Yes		Yes		< 2% Application Processor load using on-chip Digital Motion Processor (DMP). Reduces processing requirements for embedded applications
9-Axis MotionFusion	Yes		No		
Gyro Bias Calibration	Yes		Yes		No-Motion calibration and temperature calibration
3 <sup>rd</sup> Party Compass Cal API	Yes		No		Integrates 3 <sup>rd</sup> party compass libraries
Gyro-Assisted Compass Calibration (Fast Heading)	Yes		No		Quick compass calibration using gyroscope
Magnetic Anomaly Rejection (Improved Heading)	Yes		No		Uses gyro heading data when magnetic anomaly is detected



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The table below lists recommended documentation for the MotionApps software solutions.

### Software Documentation

Platform	MotionApps and MotionApps Lite	Embedded MotionApps and Embedded MotionApps Lite
<b>Software Documentation</b>	<ul style="list-style-type: none"><li>• Installation Guide for Linux and Android MotionApps Platform, v1.9 or later</li><li>• MPL Functional Specifications</li></ul>	<ul style="list-style-type: none"><li>• Embedded MotionApps Platform User Guide, v3.0 or later</li><li>• Embedded MPL Functional Specifications</li></ul>

For more information about the InvenSense MotionApps Platform, please visit the Developer's Corner or consult your local InvenSense Sales Representative.

### 1.5 Applications

- Motion-based remote controls and mice
- Pointing-based gaming
- *BlurFree*<sup>™</sup> technology (for Video/Still Image Stabilization)
- "No Touch" UI
- Health and sports monitoring
- Improved camera image quality through image stabilization
- Robotics
- Power Management

## 2 Features

The IDG/IXZ-21X0 dual axis MEMS gyroscope includes a wide range of features:

### 2.1 Sensors

- Digital-output X/Y Axis (IDG-21X0) or X/Z Axis (IXZ-21X0) angular rate sensors (gyros) on one integrated circuit
- Digital-output temperature sensor
- Factory-calibrated scale factor
- High cross-axis isolation via proprietary MEMS design
- 10,000g shock tolerant

### 2.2 Digital Output

- Fast Mode (400kHz) I<sup>2</sup>C serial interface
- 1MHz SPI (IDG/IXZ-2100 only) to access gyro and temp sensor registers only; aimed at higher speed applications which need raw data, refer to Section 5.4 for further explanation
- 16-bit ADCs for digitizing sensor outputs
- Angular rate sensors (gyros) with user-programmable full-scale-range of  $\pm 250^\circ/\text{sec}$ ,  $\pm 500^\circ/\text{sec}$ ,  $\pm 1000^\circ/\text{sec}$ , or  $\pm 2000^\circ/\text{sec}$ .

### 2.3 Data Processing

- FIFO buffers complete data set, reducing timing requirements on the system processor and saving power by letting the processor burst read the FIFO data, and then go into a low-power sleep mode while the device collects more data.
- Data collection polled or interrupt driven with on-chip programmable interrupt functionality
- Programmable low-pass filters

### 2.4 Clocking

- On-chip timing generator clock frequency  $\pm 1\%$  variation over full temperature range
- Optional external clock inputs of 32.768kHz or 19.2MHz
- 1MHz clock output

### 2.5 Power

- VDD analog supply voltage range of 2.1V to 3.6V
- Flexible VLOGIC reference voltage allows for multiple I<sup>2</sup>C interface voltages (IDG/IXZ-2150 only)
- Power consumption with both axes active: 4.5mA
- Sleep mode: 5 $\mu$ A
- Each axis can be individually powered down

### 2.6 Package

- 4x4x0.9mm QFN plastic package
- MEMS structure hermetically sealed and bonded at wafer level
- RoHS and Green compliant



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### 3 Electrical Characteristics

#### 3.1 Sensor Specifications

Typical Operating Circuit of Section 4.2, VDD = 2.5V, VLOGIC = 2.5V (IDG/IXZ-2150 only), T<sub>A</sub>=25°C.

Parameter	Conditions	Min	Typical	Max	Unit	Notes
<b>GYRO SENSITIVITY</b>						
Full-Scale Range	FS_SEL=0		±250		%s	4
	FS_SEL=1		±500			
	FS_SEL=2		±1000			
	FS_SEL=3		±2000			
Gyro ADC Word Length			16		bits	3
Sensitivity Scale Factor	FS_SEL=0		131		LSB/(°/s)	1
	FS_SEL=1		65.5			
	FS_SEL=2		32.8			
	FS_SEL=3		16.4			
Sensitivity Scale Factor Tolerance	25°C	-3		+3	%	1
Sensitivity Scale Factor Variation Over Temperature			±2		%	7
Nonlinearity	Best fit straight line; 25°C		0.2		%	6
Cross-Axis Sensitivity			2		%	6
<b>GYRO ZERO-RATE OUTPUT (ZRO)</b>						
Initial ZRO Tolerance	25°C		±20		%s	1
ZRO Variation Over Temperature			±0.1		%s/°C	7
Power-Supply Sensitivity (1-10Hz)	Sine wave, 100mVpp; VDD=2.2V		0.2		%s	5
Power-Supply Sensitivity (10 - 250Hz)	Sine wave, 100mVpp; VDD=2.2V		0.2		%s	5
Power-Supply Sensitivity (250Hz - 100kHz)	Sine wave, 100mVpp; VDD=2.2V		4		%s	5
Linear Acceleration Sensitivity	Static		0.1		%s/g	6
<b>GYRO NOISE PERFORMANCE</b>						
Total RMS Noise	FS_SEL=0 DLPFCFG=2 (100Hz)		0.1		%s-rms	1
Rate Noise Spectral Density	At 10Hz		0.01		%s/√Hz	3
<b>GYRO MECHANICAL FREQUENCIES</b>						
X-Axis		30	33	36	kHz	1
Y-Axis (IDG-21X0 only)		27	30	33	kHz	1
Z-Axis (IXZ-21X0 only)		24	27	30	kHz	1
<b>GYRO START-UP TIME</b>						
ZRO Settling	DLPFCFG=0 to ±1% of Final		50		ms	5
<b>TEMPERATURE SENSOR</b>						
Range			-30 to 85		°C	2
Sensitivity	Untrimmed		280		LSB/°C	2
Room-Temperature Offset	35°C		-13200		LSB	1
Linearity	Best fit straight line (-30°C to +85°C)		±1		°C	2
<b>TEMPERATURE RANGE</b>						
Specified Temperature Range		-40		85	°C	2

#### Notes:

1. Tested in production
2. Based on characterization of 30 parts over temperature on evaluation board or in socket
3. Based on design, through modeling, and simulation across PVT
4. Typical. Randomly selected part measured at room temperature on evaluation board or in socket
5. Based on characterization of 5 parts over temperature
6. Tested on 20 parts at room temperature
7. Based on characterization of 48 parts on evaluation board or in socket



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### 3.2 Electrical Specifications

Typical Operating Circuit of Section 4.2, VDD = 2.5V, VLOGIC=2.5V (IDG/IXZ-2150 only), T<sub>A</sub> = 25°C.

Parameters	Conditions	Min	Typical	Max	Units	Notes
<b>VDD POWER SUPPLY</b>						
Operating Voltage Range	Monotonic ramp. Ramp rate is 10% to 90% of the final value (see Figure in Section 4.4)	2.1		3.6	V	2
Power-Supply Ramp Rate		0		5	ms	2
Normal Operating Current			4.5		6.5	mA
Sleep Mode Current			5		μA	4
<b>VLOGIC REFERENCE VOLTAGE</b> (must be regulated)						
Voltage Range	VLOGIC must be ≤VDD at all times	1.71		VDD	V	3, 5
Power-Supply Ramp Rate	Monotonic ramp. Ramp rate is 10% to 90% of the final value (see Figure in Section 4.4)			1	ms	3, 5
Normal Operating Current			100		μA	4
<b>START-UP TIME FOR REGISTER READ/WRITE</b>						
			20	100	ms	4
<b>I<sup>2</sup>C ADDRESS</b>						
	AD0 = 0		1101000			1
	AD0 = 1		1101001			1
<b>DIGITAL INPUTS (SDI, SCLK, ADO, /CS, CLKIN)</b>						
V <sub>IH</sub> , High Level Input Voltage	(IDG/IXZ-2100)	0.7*VDD			V	5
V <sub>IL</sub> , Low Level Input Voltage	(IDG/IXZ-2100)			0.3*VDD	V	5
V <sub>IH</sub> , High Level Input Voltage	(IDG/IXZ-2150)	0.7*VLOGIC			V	5
V <sub>IL</sub> , Low Level Input Voltage	(IDG/IXZ/2150)			0.3*VLOGIC	V	5
C <sub>I</sub> , Input Capacitance			< 5		pF	6
<b>DIGITAL OUTPUT (INT, SDO)</b>						
V <sub>OH</sub> , High Level Output Voltage	R <sub>LOAD</sub> =1MΩ (IDG/IXZ-2100)	0.9*VDD			V	2
V <sub>OL1</sub> , LOW-Level Output Voltage	R <sub>LOAD</sub> =1MΩ (IDG/IXZ-2100)			0.1*VDD	V	2
V <sub>OH</sub> , High Level Output Voltage	R <sub>LOAD</sub> =1MΩ (IDG/IXZ-2150)	0.9*VLOGIC			V	2
V <sub>OL1</sub> , LOW-Level Output Voltage	R <sub>LOAD</sub> =1MΩ (IDG/IXZ-2150)			0.1*VLOGIC	V	2
V <sub>OL,INT1</sub> , INT Low-Level Output Voltage	OPEN=1, 0.3mA sink current			0.1	V	2
Output Leakage Current	OPEN=1		100		nA	4
t <sub>INT</sub> , INT Pulse Width	LATCH_INT_EN=0		50		μs	4
<b>DIGITAL OUTPUT (CLKOUT)</b>						
V <sub>OH</sub> , High Level Output Voltage	R <sub>LOAD</sub> =1MΩ	0.9*VDD			V	2
V <sub>OL1</sub> , LOW-Level Output Voltage	R <sub>LOAD</sub> =1MΩ			0.1*VDD	V	2

#### Notes:

1. Tested in production
2. Based on characterization of 30 parts over temperature on evaluation board or in socket
3. Typical. Randomly selected part measured at room temperature on evaluation board or in socket
4. Based on characterization of 5 parts over temperature
5. Refer to Section 4.4 for the recommended power-on procedure
6. Guaranteed by design



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### 3.3 Electrical Specifications, continued

Typical Operating Circuit of Section 4.2, VDD = 2.5V, VLOGIC = 2.5V (IDG/IXZ-2150 only), T<sub>A</sub>=25°C.

Parameters	Conditions	Typical	Units	Notes
<b>I<sup>2</sup>C I/O (SCL, SDA)</b>				
V <sub>IL</sub> , LOW-Level Input Voltage	(IDG/IXZ-2100)	-0.5 to 0.3*VDD	V	1
V <sub>IH</sub> , HIGH-Level Input Voltage	(IDG/IXZ-2100)	0.7*VDD to VDD + 0.5V	V	1
V <sub>hys</sub> , Hysteresis	(IDG/IXZ-2100)	0.1*VDD	V	1
V <sub>IL</sub> , LOW Level Input Voltage	(IDG/IXZ-2150)	-0.5V to 0.3*VLOGIC	V	1
V <sub>IH</sub> , HIGH-Level Input Voltage	(IDG/IXZ-2150)	0.7*VLOGIC to VLOGIC + 0.5V	V	1
V <sub>hys</sub> , Hysteresis	(IDG/IXZ-2150)	0.1*VLOGIC	V	1
V <sub>OL1</sub> , LOW-Level Output Voltage	3mA sink current	0 to 0.4	V	1
I <sub>OL</sub> , LOW-Level Output Current	V <sub>OL</sub> = 0.4V	3	mA	1
	V <sub>OL</sub> = 0.6V	5	mA	1
Output Leakage Current		100	nA	2
t <sub>of</sub> , Output Fall Time from V <sub>IHmax</sub> to V <sub>ILmax</sub>	C <sub>b</sub> bus capacitance in pF	20+0.1C <sub>b</sub> to 250	ns	1
C <sub>I</sub> , Capacitance for Each I/O pin		< 10	pF	3

#### Notes:

1. Based on characterization of 5 parts over temperature
2. Typical. Randomly selected part measured at room temperature on evaluation board or in socket
3. Guaranteed by design



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**3.4 Electrical Specifications, continued**

Typical Operating Circuit of Section 4.2, VDD = 2.5V, VLOGIC = 2.5V (IDG/IXZ-2150 only), T<sub>A</sub>=25°C.

Parameters	Conditions	Min	Typical	Max	Units	Notes
<b>INTERNAL CLOCK SOURCE</b>						
Sample Rate, Fast	CLK_SEL=0,1,2,3 DLPFCFG=0 SAMPLERATEDIV = 0		8		kHz	3
Sample Rate, Slow	DLPFCFG=1,2,3,4,5, or 6 SAMPLERATEDIV = 0		1		kHz	3
Reference Clock Output	CLKOUTEN = 1		1.024		MHz	3
Clock Frequency Initial Tolerance	CLK_SEL=0, 25°C	-5		+5	%	1
	CLK_SEL=1,2,3; 25°C	-1		+1	%	1
Frequency Variation over Temperature	CLK_SEL=0		-15 to +10		%	2
	CLK_SEL=1,2,3		±1		%	2
PLL Settling Time	CLK_SEL=1,2,3		1		ms	4
<b>EXTERNAL 32.768kHz CLOCK</b>						
External Clock Frequency	CLK_SEL=4		32.768		kHz	4
External Clock Jitter	Cycle-to-cycle rms		1 to 2		µs	4
Sample Rate, Fast	DLPFCFG=0 SAMPLERATEDIV = 0		8.192		kHz	4
Sample Rate, Slow	DLPFCFG=1,2,3,4,5, or 6 SAMPLERATEDIV = 0		1.024		kHz	4
Reference Clock Output	CLKOUTEN = 1		1.0486		MHz	4
PLL Settling Time			1		ms	4
<b>EXTERNAL 19.2MHz CLOCK</b>						
External Clock Frequency	CLK_SEL=5		19.2		MHz	4
Sample Rate, Fast	DLPFCFG=0 SAMPLERATEDIV = 0		8		kHz	4
Sample Rate, Slow	DLPFCFG=1,2,3,4,5, or 6 SAMPLERATEDIV = 0		1		kHz	4
Reference Clock Output	CLKOUTEN = 1		1.024		MHz	4
PLL Settling Time			1		ms	4

**Notes:**

1. Tested in production
2. Based on characterization of 30 parts over temperature on evaluation board or in socket
3. Typical. Randomly selected part measured at room temperature on evaluation board or in socket
4. Based on design, through modeling, and simulation across PVT

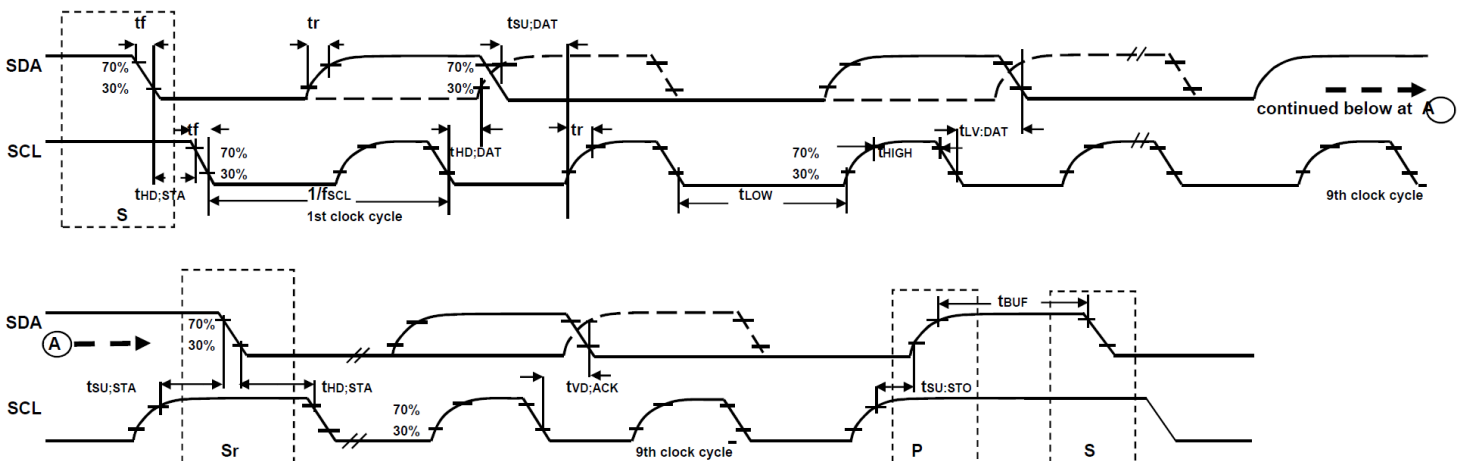
### 3.5 I<sup>2</sup>C Timing Characterization

Typical Operating Circuit of Section 4.2, VDD = 2.5V, VLOGIC = 1.8V±5% (IDG/IXZ-2150 only), 2.5V±5%, 3.0V±5%, or 3.3V±5%, T<sub>A</sub>=25°C.

Parameters	Conditions	Min	Typical	Max	Units	Notes
<b>I<sup>2</sup>C TIMING</b>						
<b>I<sup>2</sup>C FAST-MODE</b>						
f <sub>SCL</sub> , SCL Clock Frequency		0		400	kHz	1
t <sub>HD,STA</sub> , (Repeated) START Condition Hold Time		0.6			μs	1
t <sub>LOW</sub> , SCL Low Period		1.3			μs	1
t <sub>HIGH</sub> , SCL High Period		0.6			μs	1
t <sub>SU,STA</sub> , Repeated START Condition Setup Time		0.6			μs	1
t <sub>HD,DAT</sub> , SDA Data Hold Time		0			μs	1
t <sub>SU,DAT</sub> , SDA Data Setup Time		100			ns	1
t <sub>r</sub> , SDA and SCL Rise Time	C <sub>b</sub> bus cap. from 10 to 400pF	20+0.1C <sub>b</sub>		300	ns	1
t <sub>f</sub> , SDA and SCL Fall Time	C <sub>b</sub> bus cap. from 10 to 400pF	20+0.1C <sub>b</sub>		300	ns	1
t <sub>SU,STO</sub> , STOP Condition Setup Time		0.6			μs	1
t <sub>BUF</sub> , Bus Free Time Between STOP and START Condition		1.3			μs	1
C <sub>b</sub> , Capacitive Load for each Bus Line			< 400		pF	3
t <sub>VD,DAT</sub> , Data Valid Time				0.9	μs	1
t <sub>VD,ACK</sub> , Data Valid Acknowledge Time				0.9	μs	1

**Notes:**

1. Based on characterization of 5 parts over temperature on evaluation board or in socket
2. S = Start Condition, P = Stop Condition, S<sub>r</sub> = Repeated Start Condition
3. Guaranteed by design



**I<sup>2</sup>C Bus Timing Diagram**

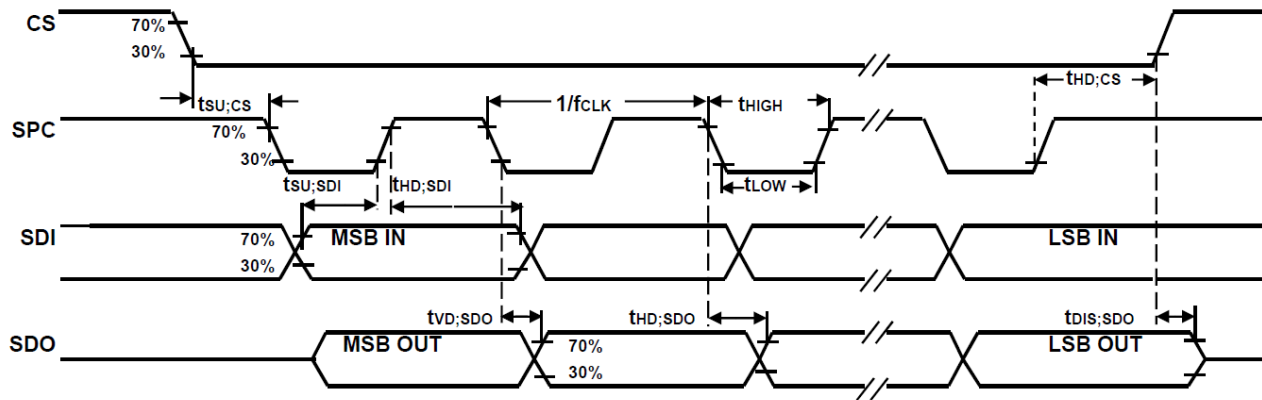
**3.6 SPI Timing Characterization (IDG/IXZ-2100 only)**

Typical Operating Circuit of Section 4.2, VDD = 2.1V to 3.6V, T<sub>A</sub> = -40°C to +85°C, unless otherwise noted. Typical values are at T<sub>A</sub>=25°C.

Parameters	Conditions	Min	Typical	Max	Units
<b>SPI TIMING</b>					
f <sub>SCLK</sub> , SCLK Clock Frequency		0.9		1	MHz
t <sub>LOW</sub> , SCLK Low Period		400			ns
t <sub>HIGH</sub> , SCLK High Period		400			ns
t <sub>SU,CS</sub> , CS Setup Time		8			ns
t <sub>HD,CS</sub> , CS Hold Time		500			ns
t <sub>SU,SDI</sub> , SDI Setup Time		11			ns
t <sub>HD,SDI</sub> , SDI Hold Time		7			ns
t <sub>VD,SDO</sub> , SDO Valid Time	C <sub>load</sub> = 20pF			100	ns
t <sub>HD,SDO</sub> , SDO Hold Time	C <sub>load</sub> = 20pF	4			ns
t <sub>DIS,SDO</sub> , SDO Output Disable Time				10	ns

**Note:**

1. Based on characterization of 5 parts over temperature as mounted on evaluation board or in sockets



**SPI Bus Timing Diagram**



### 3.7 Absolute Maximum Ratings

Stress above those listed as “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to the absolute maximum ratings conditions for extended periods may affect device reliability.

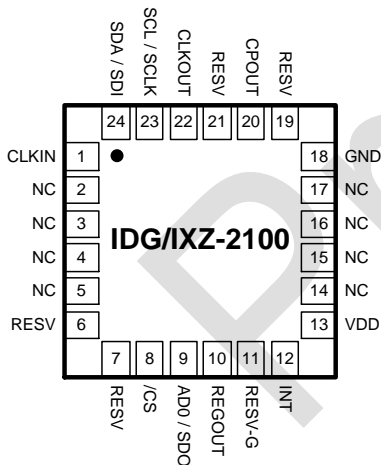
#### Absolute Maximum Ratings

Parameter	Rating
Supply Voltage, VDD	-0.5V to +6V
VLOGIC Input Voltage Level (IDG/IXZ-2150)	-0.5V to VDD + 0.5V
REGOUT	-0.5V to 2V
Input Voltage Level (CLKIN, AD0, INT, SCL, SDA)	-0.5V to VDD + 0.5V
CPOUT (2.1V ≤ VDD ≤ 3.6V )	-0.5V to 30V
Acceleration (Any Axis, unpowered)	10,000g for 0.3ms
Operating Temperature Range	-40°C to +105°C
Storage Temperature Range	-40°C to +125°C
Electrostatic Discharge (ESD) Protection	1.5kV (HBM); 200V (MM)
Latch-up	JEDEC Class II (2), 125°C Level B, ±60mA

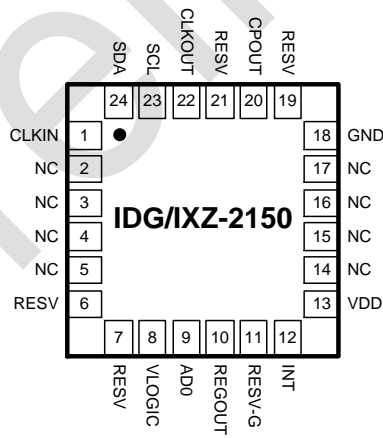
## 4 Applications Information

### 4.1 Pin Out and Signal Description

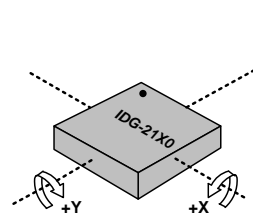
Pin Number	IDG/IXZ-2100	IDG/IXZ-2150	Pin Name	Pin Description
1	Y	Y	CLKIN	External reference clock input. Connect to GND if unused.
6	Y	Y	RESV	Reserved. Do not connect.
7	Y	Y	RESV	Reserved. Do not connect.
8	Y		/CS	SPI chip select (0=SPI mode, 1= I <sup>2</sup> C mode)
8		Y	VLOGIC	Digital I/O supply voltage. VLOGIC must be ≤ VDD at all times.
9	Y		AD0 / SDO	I <sup>2</sup> C Slave Address LSB (AD0); SPI serial data output (SDO)
9		Y	AD0	I <sup>2</sup> C Slave Address LSB
10	Y	Y	REGOUT	Regulator filter capacitor connection
11	Y	Y	RESV_G	Reserved – Connect to Ground
12	Y	Y	INT	Interrupt digital output (totem pole or open-drain)
13	Y	Y	VDD	Power supply voltage and Digital I/O supply voltage
18	Y	Y	GND	Power supply ground
19	Y	Y	RESV	Reserved. Do not connect.
20	Y	Y	CPOUT	Charge pump capacitor connection
21	Y	Y	RESV	Reserved. Do not connect.
22	Y	Y	CLKOUT	1MHz clock output for third-party accelerometer synchronization
23	Y		SCL / SCLK	I <sup>2</sup> C serial clock (SCL); SPI serial clock (SCLK)
23		Y	SCL	I <sup>2</sup> C serial clock
24	Y		SDA / SDI	I <sup>2</sup> C serial data (SDA); SPI serial data input (SDI)
24		Y	SDA	I <sup>2</sup> C serial data
2, 3, 4, 5, 14, 15, 16, 17	Y	Y	NC	Not internally connected. May be used for PCB trace routing.



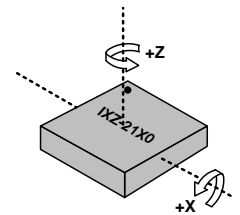
**QFN Package (Top View)**  
24-pin, 4mm x 4mm x 0.9mm



**QFN Package (Top View)**  
24-pin, 4mm x 4mm x 0.9mm

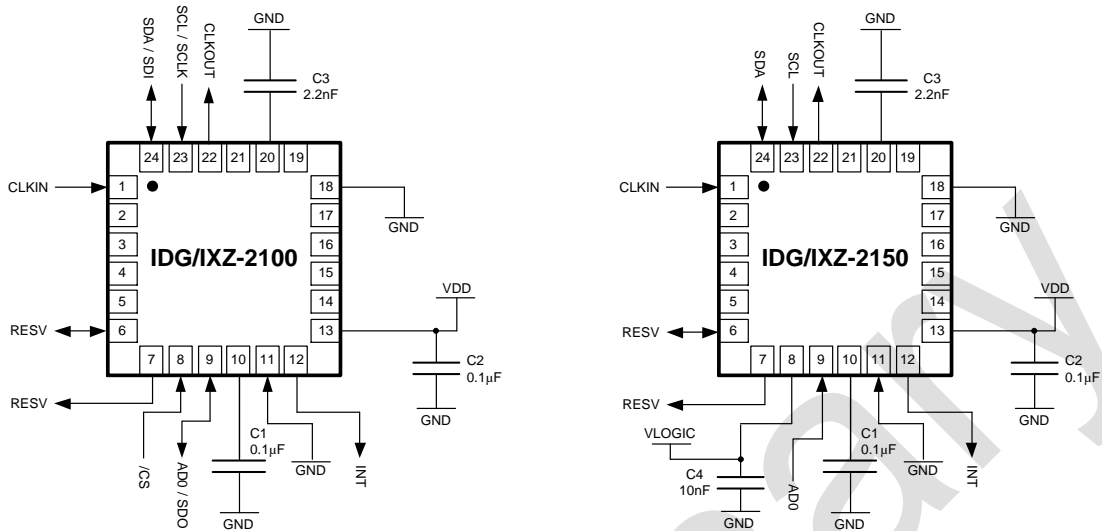


**Orientation of Axes of Sensitivity and Polarity of Rotation for IDG-21X0**



**Orientation of Axes of Sensitivity and Polarity of Rotation for IXZ-21X0**

### 4.2 Typical Operating Circuits



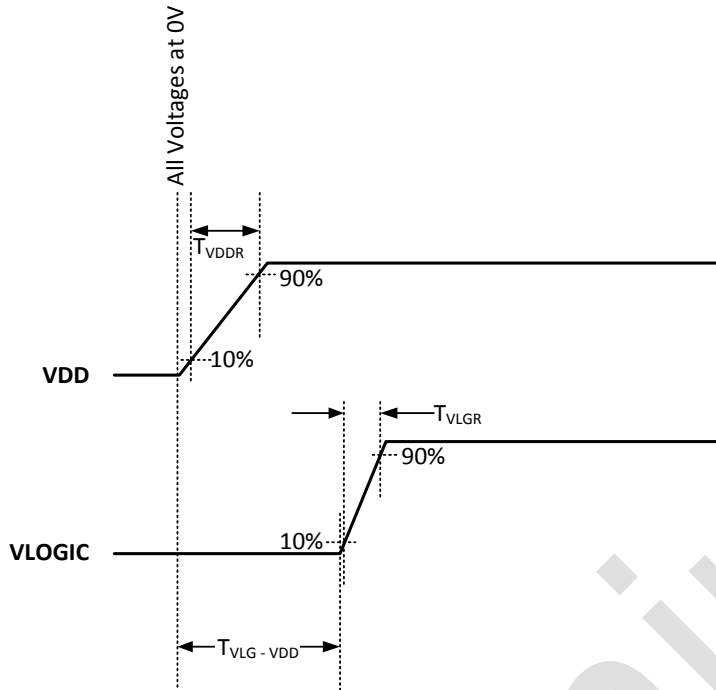
**Typical Operating Circuits**

### 4.3 Bill of Materials for External Components

Component	Label	Specification	Quantity
Regulator Filter Capacitor	C1	Ceramic, X7R, 0.1µF ±10%, 2V	1
VDD Bypass Capacitor	C2	Ceramic, X7R, 0.1µF ±10%, 4V	1
Charge Pump Capacitor	C3	Ceramic, X7R, 2.2nF ±10%, 50V	1
VLOGIC Bypass Capacitor	C4*	Ceramic, X7R, 10nF ±10%, 4V	1

\* IDG/IXZ-2150 only

#### 4.4 Recommended Power-on Procedure

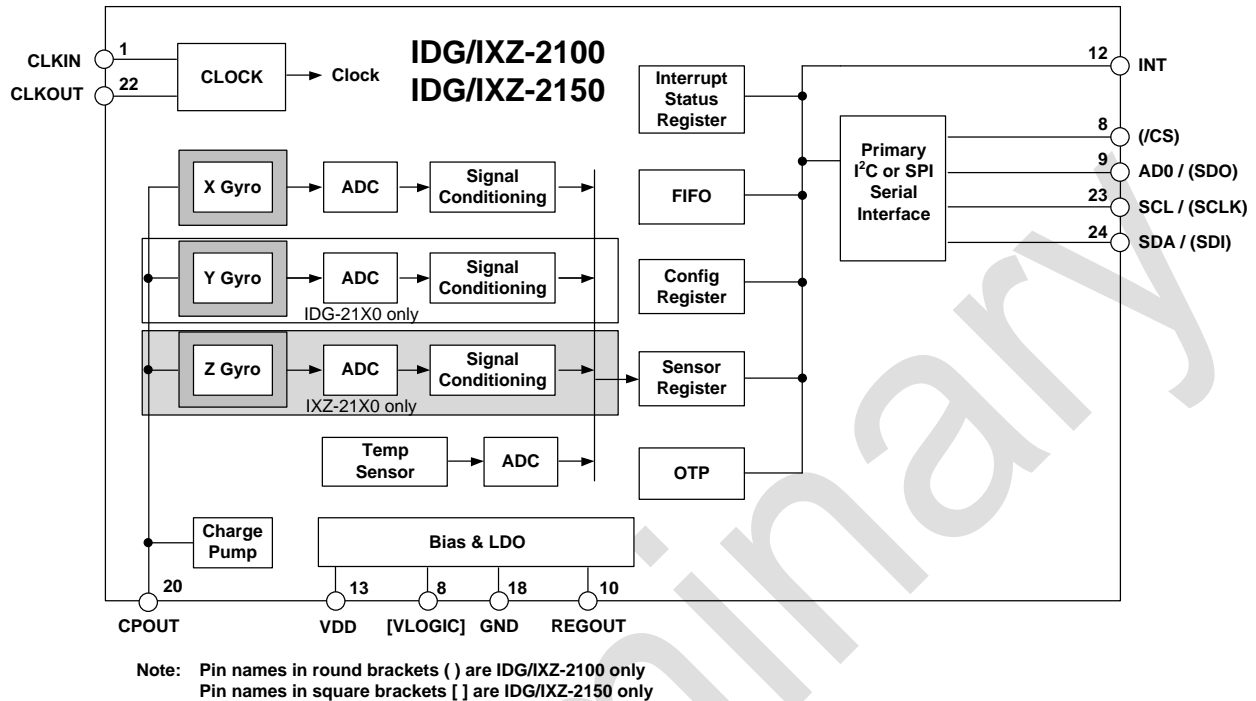


#### Power-Up Sequencing

1.  $T_{VDDR}$  is VDD rise time: Time for VDD to rise from 10% to 90% of its final value
2.  $T_{VDDR}$  is  $\leq 5\text{ms}$
3.  $T_{VLGR}$  is VLOGIC rise time: Time for VLOGIC to rise from 10% to 90% of its final value
4.  $T_{VLGR}$  is  $\leq 1\text{ms}$
5.  $T_{VLG-VDD}$  is the delay from the start of VDD ramp to the start of VLOGIC rise
6.  $T_{VLG-VDD}$  is  $\geq 0\text{ms}$ ; VLOGIC amplitude must always be  $\leq$  VDD amplitude
7. VDD and VLOGIC must be monotonic ramps

## 5 Functional Overview

### 5.1 Block Diagram



### 5.2 Overview

The IDG/IXZ-2100 and IDG/IXZ-2150 are comprised of the following key blocks / functions:

- Two-axis MEMS rate gyroscope sensors with 16-bit ADCs and signal conditioning
- Serial I<sup>2</sup>C and SPI (IDG/IXZ-2100 only) serial communications interfaces
- Clocking
- Sensor Data Registers
- FIFO
- Interrupts
- Digital-Output Temperature Sensor
- Bias and LDO
- Charge Pump

### 5.3 Two-Axis MEMS Gyroscope with 16-bit ADCs and Signal Conditioning

The IDG/IXZ-2100 and IDG/IXZ-2150 consist of two independent vibratory MEMS rate gyroscopes, which detect rotation about the X, Y, and Z axes. When the gyros are rotated about any of the sense axes, the Coriolis Effect causes a vibration that is detected by a capacitive pickoff. The resulting signal is amplified, demodulated, and filtered to produce a voltage that is proportional to the angular rate. This voltage is digitized using individual on-chip 16-bit Analog-to-Digital Converters (ADCs) to sample each axis. The full-scale range of the gyro sensors may be digitally programmed to  $\pm 250$ ,  $\pm 500$ ,  $\pm 1000$ , or  $\pm 2000$  degrees per second (dps). ADC sample rate is programmable from 8,000 samples per second, down to 3.9 samples per second, and user-selectable low-pass filters enable a wide range of cut-off frequencies.

### 5.4 I<sup>2</sup>C and SPI Serial Communications Interfaces

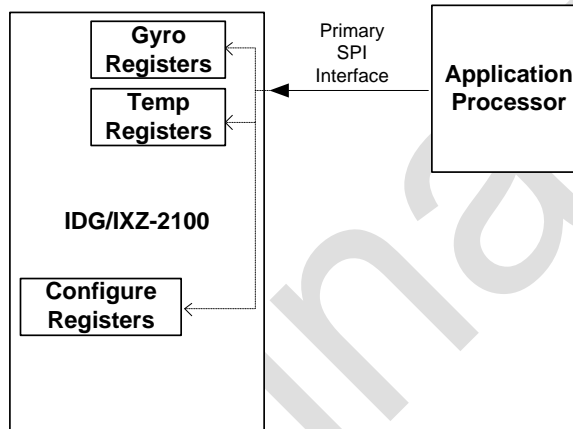
The IDG/IXZ-2100 and IDG/IXZ-2150 have an I<sup>2</sup>C serial interface and the IDG/IXZ-2100 also supports SPI protocol on the interface. SPI interface can be used to read/write to all the registers of the IDG/IXZ-2100, but the device's FIFO is not accessible via the SPI interface. IDG/IXZ-2100 and IDG/IXZ-2150 always act as

slaves when communicating to the system processor. The logic level for communications to the master is set by the voltage on the VLOGIC pin (IDG/IXZ-2150) or by VDD (IDG/IXZ-2100). The LSB of the of the I<sup>2</sup>C slave address is set by pin 9 (AD0).

I<sup>2</sup>C and SPI protocols are described in more detail in Section 6.

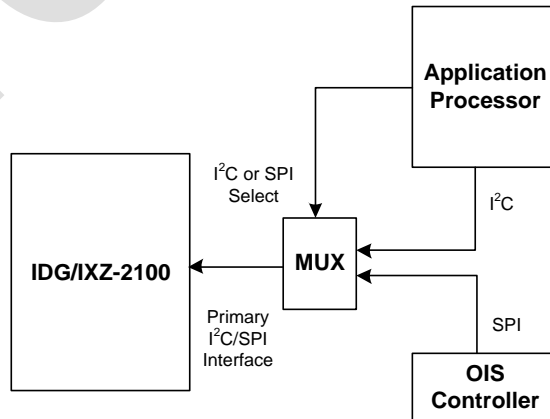
Note: When VDD is low, the I<sup>2</sup>C or SPI (IDG/IXZ-2100 only) interface pins become low impedance and thus can load the serial bus. This is a concern if other devices are active on the bus during this time.

**SPI Usage Cases (IDG/IXZ-2100 only):**



**Accessing Raw Sensor Data and Configuring IDG/IXZ-2100 using SPI interface**

The serial interface on the IDG/IXZ-2100 supports SPI protocol. This feature was designed to address high speed applications which need access to raw sensor data. As depicted in the above diagram, all the sensor registers can be accessed using the SPI interface and the IDG/IXZ-2100 can be configured through the SPI interface. The device's FIFO is not accessible via the SPI interface.



**Dual Mode Operation Using SPI**



The IDG/IXZ-2100's SPI interface can also be used in a dual-mode configuration as shown above. In this configuration, the application processor accesses all the functions of IDG/IXZ-2100 using the I<sup>2</sup>C interface of the IDG/IXZ-2100, and the OIS controller accesses only raw data from the IDG/IXZ-2100 gyroscope registers using the SPI interface. The multiplexer (MUX) is used to select which interface device is connected to the serial interface of the IDG/IXZ-2100. The figure above is simplified, since there needs to be communication between the application processor and the OIS controller, and this is not shown.

### **5.5 Internal Clock Generation**

The IDG/IXZ-2100 and IDG/IXZ-2150 have a flexible clocking scheme, allowing for a variety of internal or external clock sources for the internal synchronous circuitry. This synchronous circuitry includes the signal conditioning and ADCs and various control circuits and registers. An on-chip PLL provides flexibility in the allowable inputs for generating this clock.

Allowable internal sources for generating the internal clock are:

- An internal relaxation oscillator
- Any of the X, Y (IDG-21X- only), or Z (IXZ-21X0 only) gyros (MEMS oscillators with a drift of  $\pm 1\%$  over temperature)

Allowable external clocking sources are:

- 32.768kHz square wave
- 19.2MHz square wave

The choice of which source to select for generating the internal synchronous clock depends on the availability of external sources and the requirements for power consumption and clock accuracy. Most likely, these requirements will vary by mode of operation. For example, in a mode where the gyros are active, selecting the gyros as the clock source provides for an accurate clock source.

There are also start-up conditions to consider. When the IDG/IXZ-2100 and IDG/IXZ-2150 initially start up, the device operates off of its internal clock until programmed to operate from another source. This allows the user, for example, to wait for the MEMS oscillators to stabilize before they are selected as the clock source.

### **5.6 Clock Output**

The IDG/IXZ-2100 and IDG/IXZ-2150 provide a clock output.

### **5.7 Sensor Data Registers**

The sensor data registers contain the latest gyro and temperature data. They are read-only registers, and are accessed via the Serial Interface. Data from these registers may be read anytime. However, the interrupt function may be used to determine when new data is available.

### **5.8 FIFO**

The IDG/IXZ-2100 and IDG/IXZ-2150 contain a 512-byte FIFO register that is accessible via the Serial Interface. The FIFO configuration register determines what data goes into it, with possible choices being gyro data and temperature readings. A FIFO counter keeps track of how many bytes of valid data are contained in the FIFO. The FIFO register supports burst reads. The interrupt function may be used to determine when new data is available.

### **5.9 Interrupts**

Interrupt functionality is configured via the Interrupt Configuration register. Items that are configurable include the INT pin configuration, the interrupt latching and clearing method, and triggers for the interrupt. Items that can trigger an interrupt are (1) Clock generator locked to new reference oscillator (used when switching clock sources), and (2) new data is available to be read (from the FIFO and Data registers). The interrupt status can be read from the Interrupt Status register.

### **5.10 Digital-Output Temperature Sensor**

An on-chip temperature sensor and ADC are used to measure the IDG/IXZ-2100 and IDG/IXZ-2150 die temperature. The readings from the ADC can be read from the FIFO or the Sensor Data registers.



### **5.11 Bias and LDO**

The bias and LDO section generates the internal supply and the reference voltages and currents required by the IDG/IXZ-2100 and IDG/IXZ-2150. Its two inputs are an unregulated VDD of 2.1V to 3.6V and a VLOGIC logic reference supply voltage of 1.71V to VDD (IDG/IXZ-2150 only). The LDO output is bypassed by a 0.1 $\mu$ F capacitor at REGOUT.

### **5.12 Charge Pump**

An on-board charge pump generates the high voltage required for the MEMS oscillators. Its output is bypassed by a 2.2nF capacitor at CPOUT.

Preliminary



## 6 Digital Interface

### 6.1 I<sup>2</sup>C and SPI (IDG/IXZ-2100 only) Serial Interfaces

The internal registers of the IDG/IXZ-2100 and IDG/IXZ-2150 can be accessed using either the I<sup>2</sup>C or SPI (IDG/IXZ-2100 & raw sensor data only) interface. SPI operates in four-wire mode.

#### Serial Interface

Pin Number	IDG/IXZ-2100	IDG/IXZ-2150	Pin Name	Pin Description
8	Y		/CS	SPI chip select (0=SPI mode, I <sup>2</sup> C disable, 1= I <sup>2</sup> C mode, SPI disable)
8		Y	VLOGIC	Digital I/O supply voltage. VLOGIC must be ≤ VDD at all times.
9	Y		AD0 / SDO	I <sup>2</sup> C Slave Address LSB (AD0); SPI serial data output (SDO)
9		Y	AD0	I <sup>2</sup> C Slave Address LSB
23	Y		SCL / SCLK	I <sup>2</sup> C serial clock (SCL); SPI serial clock (SCLK)
23		Y	SCL	I <sup>2</sup> C serial clock
24	Y		SDA / SDI	I <sup>2</sup> C serial data (SDA); SPI serial data input (SDI)
24		Y	SDA	I <sup>2</sup> C serial data

#### Note 1:

To prevent switching into I<sup>2</sup>C mode when using SPI (IDG/IXZ-2100), the I<sup>2</sup>C interface should be disabled by setting the *I2C\_IF\_DIS* configuration bit in the *WHO\_AM\_I* register. Setting this bit should be performed immediately after waiting the time specified by the “Start-Up Time for Register Read/Write” in Section 3.2.

#### 6.1.1 I<sup>2</sup>C Interface

I<sup>2</sup>C is a two-wire interface comprised of the signals serial data (SDA) and serial clock (SCL). In general, the lines are open-drain and bi-directional. In a generalized I<sup>2</sup>C interface implementation, attached devices can be a master or a slave. The master device puts the slave address on the bus, and the slave device with the matching address acknowledges the master.

The IDG/IXZ-2100 and IDG/IXZ-2150 always operate as a slave device when communicating to the system processor, which thus acts as the master. SDA and SCL lines typically need pull-up resistors to VDD. The maximum bus speed is 400kHz.

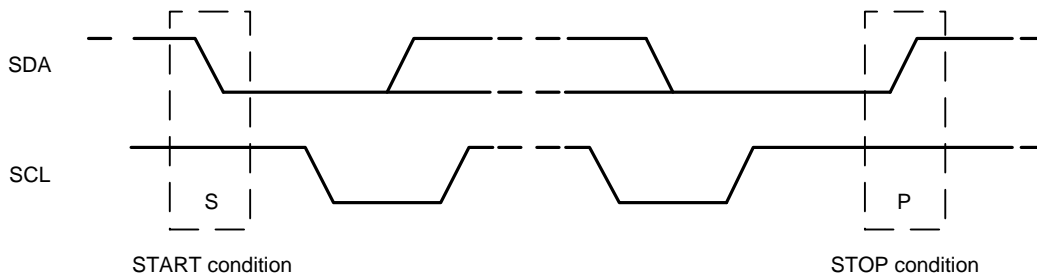
The slave address of the IDG/IXZ-2100 and IDG/IXZ-2150 is b110100X which is 7 bits long. The LSB bit of the 7 bit address is determined by the logic level on pin AD0. This allows two such devices to be connected to the same I<sup>2</sup>C bus. When used in this configuration, the address of the one of the devices should be b1101000 (pin AD0 is logic low) and the address of the other should be b1101001 (pin AD0 is logic high). The I<sup>2</sup>C address is stored in *WHO\_AM\_I* register.

#### I<sup>2</sup>C Communications Protocol

##### *START (S) and STOP (P) Conditions*

Communication on the I<sup>2</sup>C bus starts when the master puts the START condition (S) on the bus, which is defined as a HIGH-to-LOW transition of the SDA line while SCL line is HIGH (see figure below). The bus is considered to be busy until the master puts a STOP condition (P) on the bus, which is defined as a LOW to HIGH transition on the SDA line while SCL is HIGH (see figure below).

Additionally, the bus remains busy if a repeated START (Sr) is generated instead of a STOP condition.

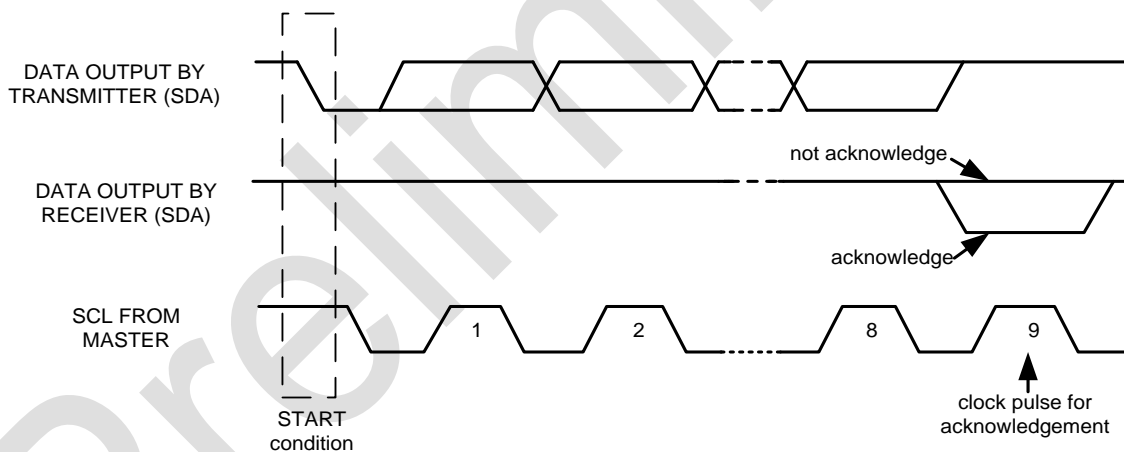


**START and STOP Conditions**

Data Format / Acknowledge

I<sup>2</sup>C data bytes are defined to be 8 bits long. There is no restriction to the number of bytes transmitted per data transfer. Each byte transferred must be followed by an acknowledge (ACK) signal. The clock for the acknowledge signal is generated by the master, while the receiver generates the actual acknowledge signal by pulling down SDA and holding it low during the HIGH portion of the acknowledge clock pulse.

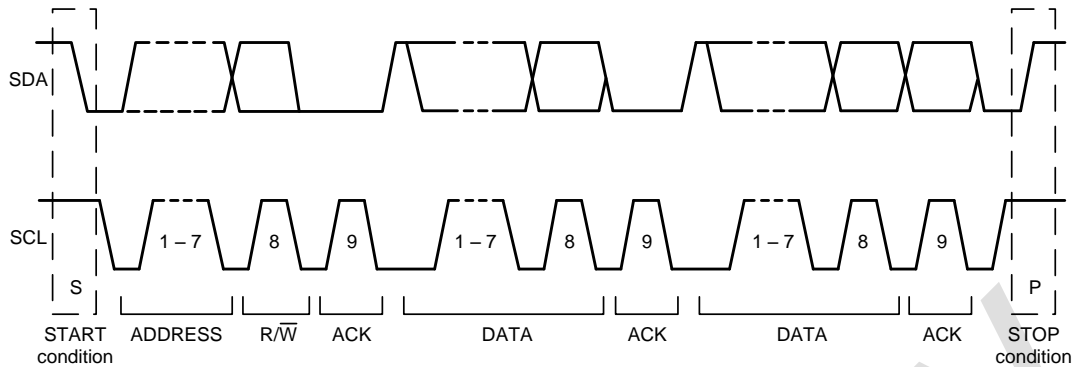
If a slave is busy and is unable to transmit or receive another byte of data until some other task has been performed, it can hold SCL LOW, thus forcing the master into a wait state. Normal data transfer resumes when the slave is ready, and releases the clock line (refer to the following figure).



**Acknowledge on the I<sup>2</sup>C Bus**

Communications

After beginning communications with the START condition (S), the master sends a 7-bit slave address followed by an 8<sup>th</sup> bit, the read/write bit. The read/write bit indicates whether the master is receiving data from or is writing to the slave device. Then, the master releases the SDA line and waits for the acknowledge signal (ACK) from the slave device. Each byte transferred must be followed by an acknowledge bit. To acknowledge, the slave device pulls the SDA line LOW and keeps it LOW for the high period of the SCL line. Data transmission is always terminated by the master with a STOP condition (P), thus freeing the communications line. However, the master can generate a repeated START condition (Sr), and address another slave without first generating a STOP condition (P). A LOW to HIGH transition on the SDA line while SCL is HIGH defines the stop condition. All SDA changes should take place when SCL is low, with the exception of start and stop conditions.



**Complete I<sup>2</sup>C Data Transfer**

To write the internal IDG/IXZ-2100 or IDG/IXZ-2150 registers, the master transmits the start condition (S), followed by the I<sup>2</sup>C address and the write bit (0). At the 9<sup>th</sup> clock cycle (when the clock is high), the IDG/IXZ-21X0 acknowledges the transfer. Then the master puts the register address (RA) on the bus. After the IDG/IXZ-21X0 acknowledges the reception of the register address, the master puts the register data onto the bus. This is followed by the ACK signal, and data transfer may be concluded by the stop condition (P). To write multiple bytes after the last ACK signal, the master can continue outputting data rather than transmitting a stop signal. In this case, the IDG/IXZ-21X0 automatically increments the register address and loads the data to the appropriate register. The following figures show single and two-byte write sequences.

**Single-Byte Write Sequence**

Master	S	AD+W		RA		DATA		P
Slave			ACK		ACK		ACK	

**Burst Write Sequence**

Master	S	AD+W		RA		DATA		DATA		P
Slave			ACK		ACK		ACK		ACK	

To read the internal IDG/IXZ-21X0 registers, the master sends a start condition, followed by the I<sup>2</sup>C address and a write bit, and then the register address that is going to be read. Upon receiving the ACK signal from the IDG/IXZ-21X0, the master transmits a start signal followed by the slave address and read bit. As a result, the IDG/IXZ-21X0 sends an ACK signal and the data. The communication ends with a not acknowledge (NACK) signal and a stop bit from master. The NACK condition is defined such that the SDA line remains high at the 9<sup>th</sup> clock cycle. The following figures show single and two-byte read sequences.

**Single-Byte Read Sequence**

Master	S	AD+W		RA		S	AD+R			NACK	P
Slave			ACK		ACK			ACK	DATA		

**Burst Read Sequence**

Master	S	AD+W		RA		S	AD+R			ACK		NACK	P
Slave			ACK		ACK			ACK	DATA		DATA		



### I<sup>2</sup>C Terms

Signal	Description
S	Start Condition: SDA goes from high to low while SCL is high
AD	Slave I <sup>2</sup> C address
W	Write bit (0)
R	Read bit (1)
ACK	Acknowledge: SDA line is low while the SCL line is high at the 9 <sup>th</sup> clock cycle
NACK	Not-Acknowledge: SDA line stays high at the 9 <sup>th</sup> clock cycle
RA	IDG/IXZ-21X0 internal register address
DATA	Transmit or received data
P	Stop condition: SDA going from low to high while SCL is high

**6.1.2 SPI interface (IDG/IXZ-2100 only)**

SPI is a 4-wire synchronous serial interface that uses two control and two data lines. The IDG/IXZ-2100 always operates as a Slave device during standard Master-Slave SPI operation. With respect to the Master, the Serial Clock output (SCLK), the Data Output (SDO) and the Data Input (SDI) are shared among the Slave devices. The Master generates an independent Chip Select (/CS) for each Slave device; /CS goes low at the start of transmission and goes back high at the end. The Serial Data Output (SDO) line, remains in a high-impedance (high-z) state when the device is not selected, so it does not interfere with any active devices.

SPI Operational Features

1. Data is delivered MSB first and LSB last
2. Data is latched on rising edge of SCLK
3. Data should be transitioned on the falling edge of SCLK
4. SCLK frequency is 1MHz max
5. SPI read and write operations are completed in 16 or more clock cycles (two or more bytes). The first byte contains the SPI Address, and the following byte(s) contain(s) the SPI data. The first bit of the first byte contains the Read/Write bit and indicates the Read (1) or Write (0) operation. The following 7 bits contain the Register Address. In cases of multiple-byte Read/Writes, data is two or more bytes:

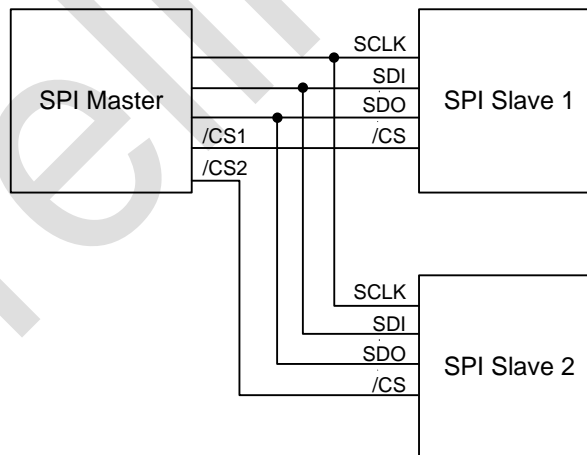
**SPI Address format**

<b>MSB</b>							<b>LSB</b>
R/W	A6	A5	A4	A3	A2	A1	A0

**SPI Data format**

<b>MSB</b>							<b>LSB</b>
D7	D6	D5	D4	D3	D2	D1	D0

6. Supports Single or Burst Read/Writes.



**Typical SPI Master / Slave Configuration**

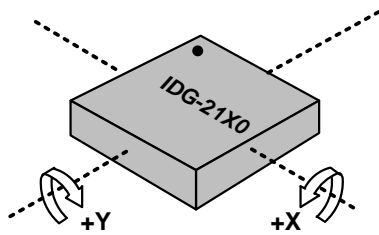
Each SPI slave requires its own Chip Select (/CS) line. SDO, SDI and SCLK lines are shared. Only one /CS line is active (low) at a time ensuring that only one slave is selected at a time. The /CS lines of other slaves are held high which causes their respective SDO pins to be high-Z.

## 7 Assembly

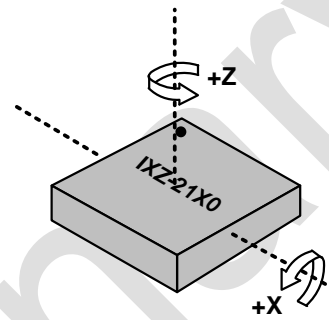
This section provides general guidelines for assembling InvenSense Micro Electro-Mechanical Systems (MEMS) gyros packaged in Quad Flat No leads package (QFN) surface mount integrated circuits.

### 7.1 Orientation of Axes

The diagram below shows the orientation of the axes of sensitivity and the polarity of rotation. Note the pin 1 identifier (•) in the figure.

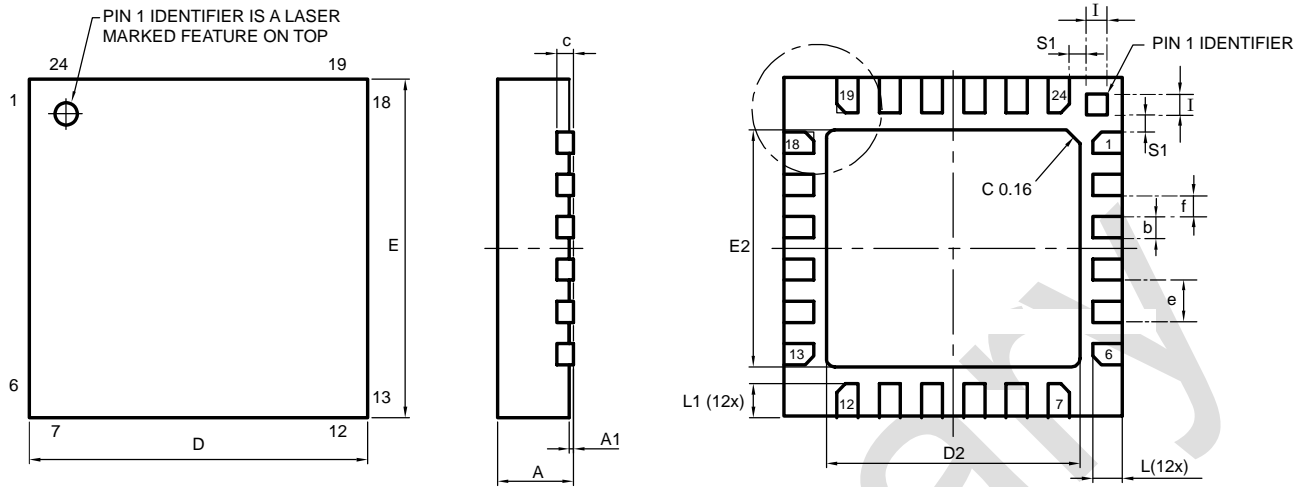


**Orientation of Axes of Sensitivity and Polarity of Rotation for IDG-21X0**

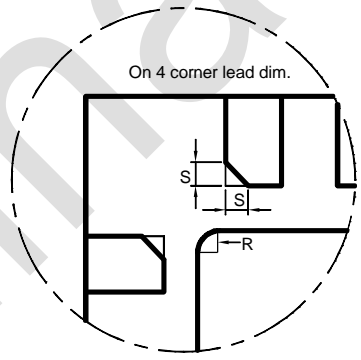


**Orientation of Axes of Sensitivity and Polarity of Rotation for IXZ-21X0**

**7.2 Package Dimensions:**

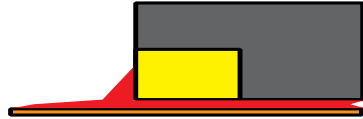


SYMBOLS	DIMENSIONS IN MILLIMETERS		
	MIN	NOM	MAX
A	0.85	0.90	0.95
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
c	---	0.20 REF.	---
D	3.90	4.00	4.10
D2	2.95	3.00	3.05
E	3.90	4.00	4.10
E2	2.75	2.80	2.85
e	---	0.50	---
f (e-b)	0.20	0.25	0.32
L	0.30	0.35	0.40
L1	0.35	0.40	0.45
l	0.20	0.25	0.30
R	0.05	---	0.10
s	0.05	---	0.15
S1	0.15	0.20	0.25

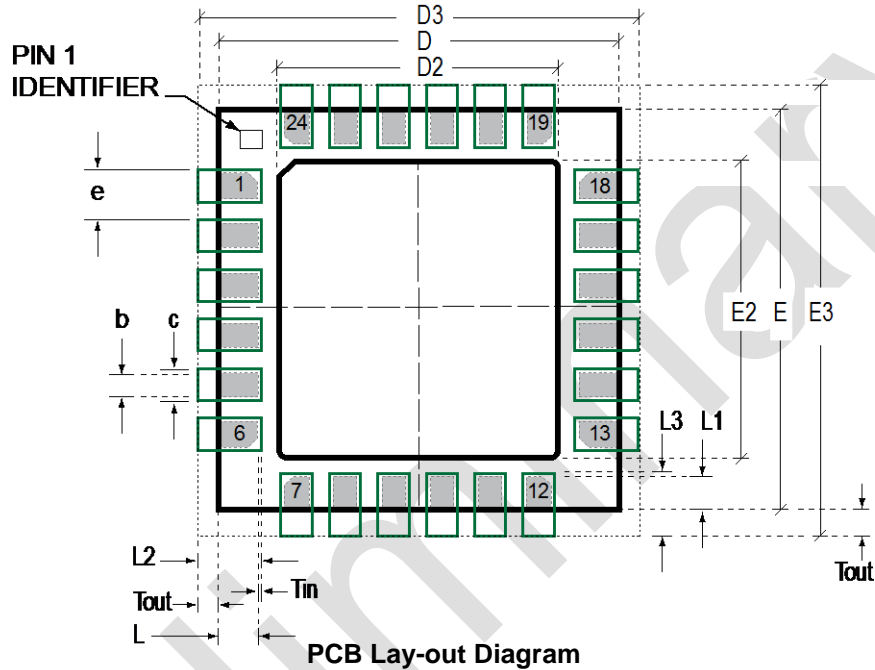


**7.3 PCB Design Guidelines:**

The Pad Diagram using a JEDEC type extension with solder rising on the outer edge is shown below. The Pad Dimensions Table shows pad sizing (mean dimensions) recommended for the IDG/IXZ-21X0 product.



JEDEC type extension with solder rising on outer edge



**PCB Lay-out Diagram**

SYMBOLS	DIMENSIONS IN MILLIMETERS	NOM
Nominal Package I/O Pad Dimensions		
e	Pad Pitch	0.50
b	Pad Width	0.25
L	Pad Length	0.35
L1	Pad Length	0.40
D	Package Width	4.00
E	Package Length	4.00
D2	Exposed Pad Width	3.00
E2	Exposed Pad Length	2.80
I/O Land Design Dimensions (Guidelines )		
D3	I/O Pad Extent Width	4.80
E3	I/O Pad Extent Length	4.80
c	Land Width	0.35
Tout	Outward Extension	0.40
Tin	Inward Extension	0.05
L2	Land Length	0.80
L3	Land Length	0.85

**PCB Dimensions Table (for PCB Lay-out Diagram)**

## 7.4 Assembly Precautions

### 7.4.1 Gyroscope Surface Mount Guidelines

InvenSense MEMS Gyros sense rate of rotation. In addition, gyroscopes sense mechanical stress coming from the printed circuit board (PCB). This PCB stress can be minimized by adhering to certain design rules:

When using MEMS gyroscope components in plastic packages, PCB mounting and assembly can cause package stress. This package stress in turn can affect the output offset and its value over a wide range of temperatures. This stress is caused by the mismatch between the Coefficient of Linear Thermal Expansion (CTE) of the package material and the PCB. Care must be taken to avoid package stress due to mounting.

Traces connected to pads should be as symmetric as possible. Maximizing symmetry and balance for pad connection will help component self alignment and will lead to better control of solder paste reduction after reflow.

Any material used in the surface mount assembly process of the MEMS gyroscope should be free of restricted RoHS elements or compounds. Pb-free solders should be used for assembly.

### 7.4.2 Exposed Die Pad Precautions

The IDG/IXZ-21X0 has very low active and standby current consumption. The exposed die pad is not required for heat sinking, and should not be soldered to the PCB. Failure to adhere to this rule can induce performance changes due to package thermo-mechanical stress. There is no electrical connection between the pad and the CMOS.

### 7.4.3 Trace Routing

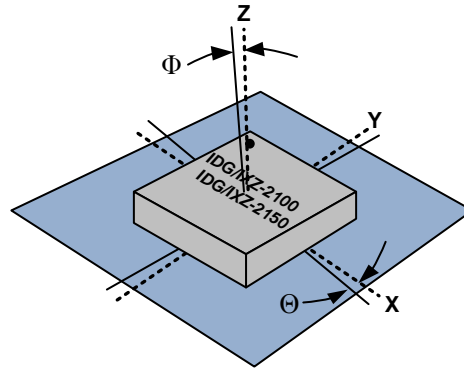
Routing traces or vias under the gyro package such that they run under the exposed die pad is prohibited. Routed active signals may harmonically couple with the gyro MEMS devices, compromising gyro response. These devices are designed with the drive frequencies as follows: X =  $33\pm 3\text{kHz}$ , Y =  $30\pm 3\text{kHz}$ , and Z =  $27\pm 3\text{kHz}$ . To avoid harmonic coupling don't route active signals in non-shielded signal planes directly below, or above the gyro package. Note: For best performance, design a ground plane under the e-pad to reduce PCB signal noise from the board on which the gyro device is mounted. If the gyro device is stacked under an adjacent PCB board, design a ground plane directly above the gyro device to shield active signals from the adjacent PCB board.

### 7.4.4 Component Placement

Do not place large insertion components such as keyboard or similar buttons, connectors, or shielding boxes at a distance of less than 6 mm from the MEMS gyro. Maintain generally accepted industry design practices for component placement near the IDG/IXZ-21X0 to prevent noise coupling and thermo-mechanical stress.

### 7.4.5 PCB Mounting and Cross-Axis Sensitivity

Orientation errors of the gyroscope mounted to the printed circuit board can cause cross-axis sensitivity in which one gyro responds to rotation about another axis. For example, the X-axis gyroscope may respond to rotation about the Y or Z axes. The orientation mounting errors are illustrated in the figure below.



**Package Gyro Axes ( - - - ) Relative to PCB Axes ( ——— ) with Orientation Errors ( $\Theta$  and  $\Phi$ )**

The table below shows the cross-axis sensitivity of the gyroscope for a given orientation error.

**Cross-Axis Sensitivity vs. Orientation Error**

Orientation Error ( $\theta$ or $\Phi$ )	Cross-Axis Sensitivity ( $\sin\theta$ or $\sin\Phi$ )
0°	0%
0.5°	0.87%
1°	1.75%

The specification for cross-axis sensitivity in Section 3.1 includes the effect of the die orientation error with respect to the package.

**7.4.6 MEMS Handling Instructions**

MEMS (Micro Electro-Mechanical Systems) are a time-proven, robust technology used in hundreds of millions of consumer, automotive and industrial products. MEMS devices consist of microscopic moving mechanical structures. They differ from conventional IC products, even though they can be found in similar packages. Therefore, MEMS devices require different handling precautions than conventional ICs prior to mounting onto printed circuit boards (PCBs).

The IDG/IXZ-21X0 gyroscope has been qualified to a shock tolerance of 10,000g. InvenSense packages its gyroscopes as it deems proper for protection against normal handling and shipping. It recommends the following handling precautions to prevent potential damage.

- Do not drop individually packaged gyroscopes, or trays of gyroscopes onto hard surfaces. Components placed in trays could be subject to g-forces in excess of 10,000g if dropped.
- Printed circuit boards that incorporate mounted gyroscopes should not be separated by manually snapping apart. This could also create g-forces in excess of 10,000g.

**7.4.7 ESD Considerations**

Establish and use ESD-safe handling precautions when unpacking and handling ESD-sensitive devices.

- Store ESD sensitive devices in ESD safe containers until ready for use. The Tape-and-Reel moisture-sealed bag is an ESD approved barrier. The best practice is to keep the units in the original moisture sealed bags until ready for assembly.
- Restrict all device handling to ESD protected work areas that measure less than 200V static charge. Ensure that all workstations and personnel are properly grounded to prevent ESD.

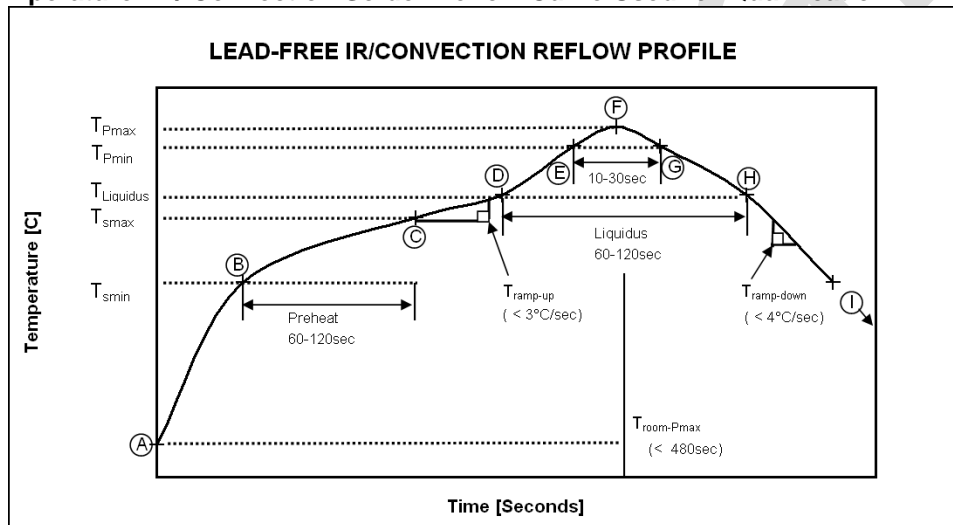
### 7.4.8 Reflow Specification

**Qualification Reflow:** The IDG/IXZ-21X0 gyroscope was qualified in accordance with IPC/JEDEC J-STD-020D.01. This standard classifies proper packaging, storage and handling in order to avoid subsequent thermal and mechanical damage during the solder reflow attachment phase of assembly. The classification specifies a sequence consisting of a bake cycle, a moisture soak cycle in a temperature humidity oven, followed by three solder reflow cycles and functional testing for qualification. All temperatures refer to the topside of the QFN package, as measured on the package body surface. The peak solder reflow classification temperature requirement is  $(260 \pm 5/-0^{\circ}\text{C})$  for lead-free soldering of components measuring less than 1.6 mm in thickness.

**Production Reflow:** Check the recommendations of your solder manufacturer. For optimum results, production solder reflow processes should reduce exposure to high temperatures, and use lower ramp-up and ramp-down rates than those used in the component qualification profile shown for reference below.

Production reflow should never exceed the maximum constraints listed in the table and shown in the figure below. These constraints were used for the qualification profile, and represent the maximum tolerable ratings for the device.

#### Maximum Temperature IR / Convection Solder Reflow Curve Used for Qualification



#### Temperature Set Points for IR / Convection Reflow Corresponding to Figure Above

Step	Setting	CONSTRAINTS		
		Temp ( $^{\circ}\text{C}$ )	Time (sec)	Rate ( $^{\circ}\text{C}/\text{sec}$ )
A	$T_{\text{room}}$	25		
B	$T_{\text{Smin}}$	150		
C	$T_{\text{Smax}}$	200	$60 < t_{\text{BC}} < 120$	
D	$T_{\text{Liquidus}}$	217		$\Gamma(T_{\text{Liquidus}}-T_{\text{Pmax}}) < 3$
E	$T_{\text{Pmin}}$ [255 $^{\circ}\text{C}$ , 260 $^{\circ}\text{C}$ ]	255		$\Gamma(T_{\text{Liquidus}}-T_{\text{Pmax}}) < 3$
F	$T_{\text{Pmax}}$ [260 $^{\circ}\text{C}$ , 265 $^{\circ}\text{C}$ ]	260	$t_{\text{AF}} < 480$	$\Gamma(T_{\text{Liquidus}}-T_{\text{Pmax}}) < 3$
G	$T_{\text{Pmin}}$ [255 $^{\circ}\text{C}$ , 260 $^{\circ}\text{C}$ ]	255	$10 < t_{\text{EG}} < 30$	$\Gamma(T_{\text{Pmax}}-T_{\text{Liquidus}}) < 4$
H	$T_{\text{Liquidus}}$	217	$60 < t_{\text{DH}} < 120$	
I	$T_{\text{room}}$	25		

Note: For users  $T_{\text{Pmax}}$  must not exceed the classification temperature (260 $^{\circ}\text{C}$ ).  
For suppliers  $T_{\text{Pmax}}$  must equal or exceed the classification temperature.



**IDG-21X0 & IXZ-21X0 Product Specification**

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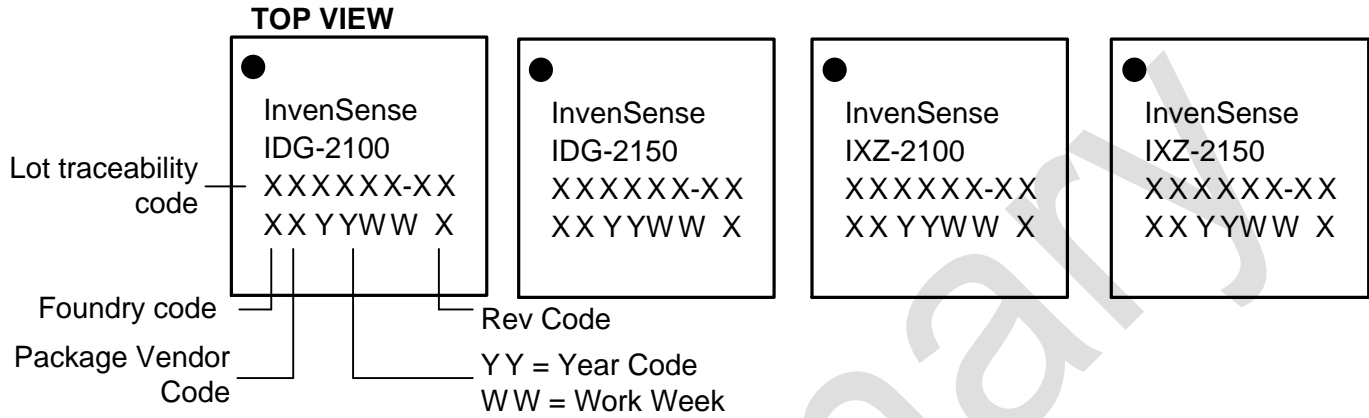
**7.4.9 Storage Specifications**

The storage specification of the IDG/IXZ-21X0 gyroscope conforms to IPC/JEDEC J-STD-020D.01 Moisture Sensitivity Level (MSL) 3.

Calculated shelf-life in moisture-sealed bag	12 months -- Storage conditions: <40°C and <90% RH
After opening moisture-sealed bag	▪ hours -- Storage conditions: ambient ≤30°C at 60%RH

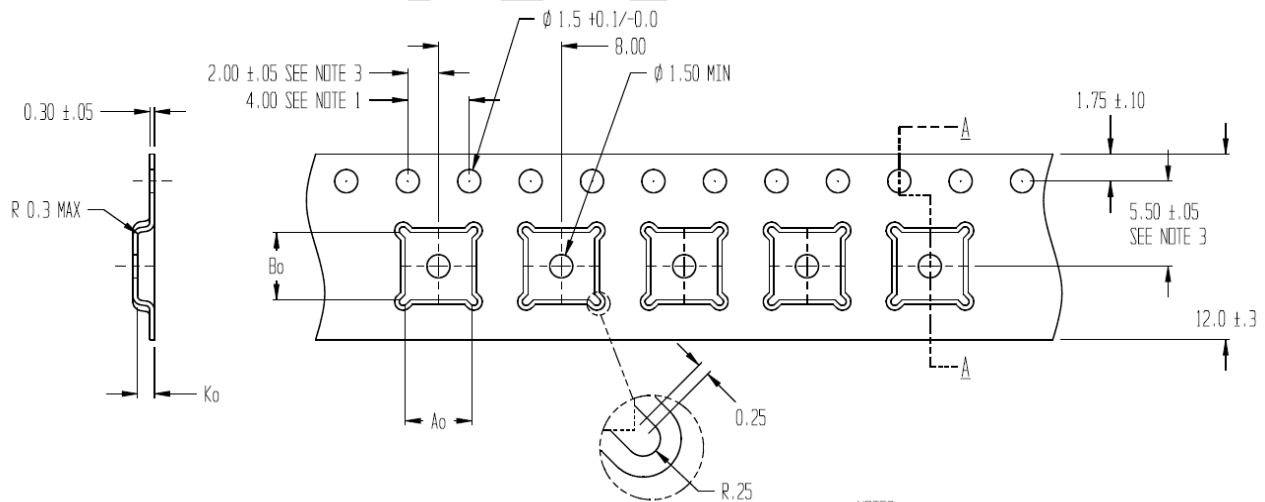
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**7.5 Package Marking Specification**



**Package Marking Specification**

**7.6 Tape & Reel Specification**



SECTION A - A

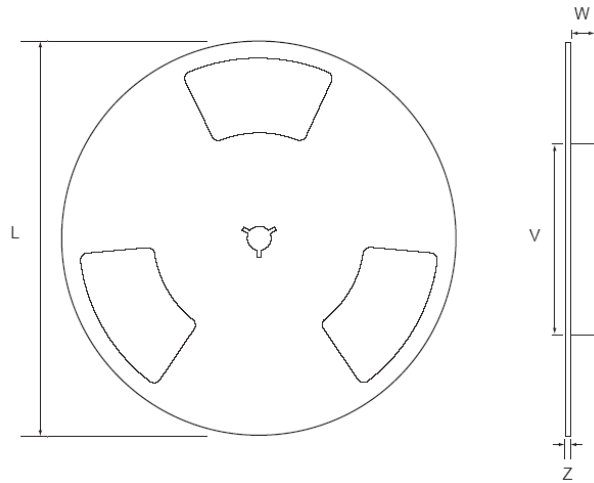
Ao = 4.35  
Bo = 4.35  
Ko = 1.1

TOLERANCES - UNLESS NOTED  
1PL ± 0.2 2PL ± 0.10

ALL DIMENSIONS IN MILLIMETERS

- NOTES:
1. 10 SPROCKET HOLE PITCH CUMULATIVE TOLERANCE ± 0.2
  2. CAMBER IN COMPLIANCE WITH EIA 481
  3. POCKET POSITION RELATIVE TO SPROCKET HOLE MEASURED AS TRUE POSITION OF POCKET, NOT POCKET HOLE

**Tape Dimensions**

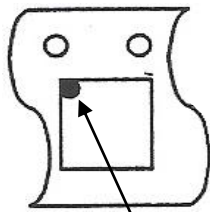


**Reel Outline Drawing**

**Reel Dimensions and Package Size**

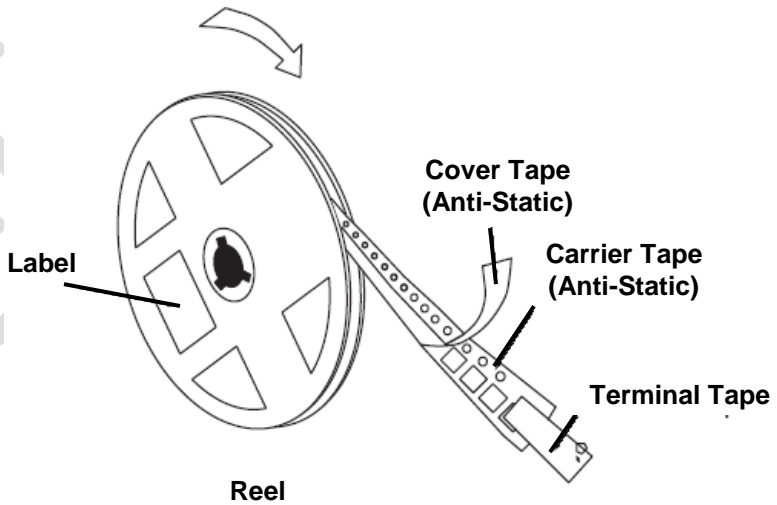
PACKAGE SIZE	REEL (mm)			
	L	V	W	Z
4x4	330	100	13.2	2.2

**Package Orientation**



Pin 1

**User Direction of Feed**



Reel

**Tape and Reel Specification**

**Reel Specifications**

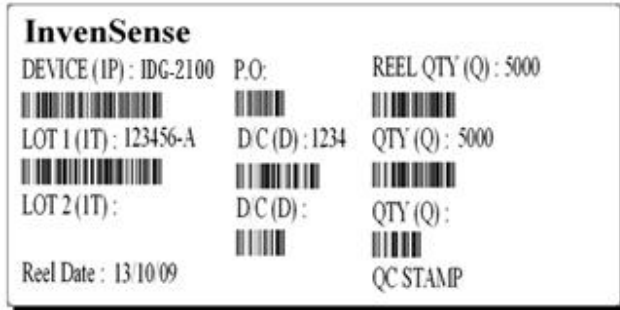
Quantity Per Reel	5,000
Reels per Box	1
Boxes Per Carton (max)	3
Pieces per Carton (max)	15,000



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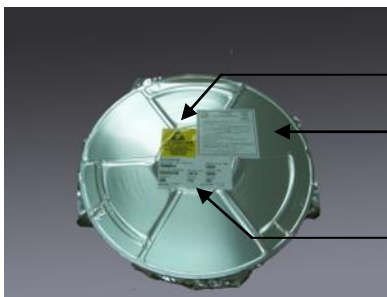
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## 7.7 Label



Location of Label

## 7.8 Packaging

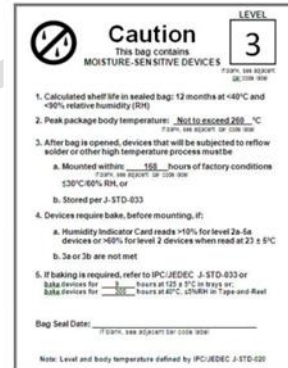


Moisture Barrier Bag With Labels

ESD Anti-static Label

Moisture-Sensitivity Caution Label

Tape & Reel Barcode Label



Moisture-Sensitivity Caution Label



Reel in Box



Box with Tape & Reel Label



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## 8 Reliability

### 8.1 Qualification Test Policy

Before InvenSense products are released for production, they complete a series of qualification tests. The Qualification Test Plan for the IDG/IXZ-21X0 followed the JEDEC JESD47G.01 Standard, "Stress-Test-Driven Qualification of Integrated Circuits." The individual tests are described below.

### 8.2 Qualification Test Plan

#### Accelerated Life Tests

TEST	Method/Condition	Lot Quantity	Sample / Lot	Acc / Reject Criteria
High Temperature Operating Life (HTOL/LFR)	JEDEC JESD22-A108C, Dynamic, 3.63V biased, $T_j > 125^\circ\text{C}$ [read-points 168, 500, 1000 hours]	3	77	(0/1)
Highly Accelerated Stress Test <sup>(1)</sup> (HAST)	JEDEC JESD22-A118 Condition A, 130°C, 85%RH, 33.3 psia., unbiased, [read-point 96 hours]	3	77	(0/1)
High Temperature Storage Life (HTS)	JEDEC JESD22-A103C, Cond. A, 125°C, Non-Biased Bake [read-points 168, 500, 1000 hours]	3	77	(0/1)

#### Device Component Level Tests

TEST	Method/Condition	Lot Quantity	Sample / Lot	Acc / Reject Criteria
ESD-HBM	JEDEC JESD22-A114F, (1.5KV)	1	3	(0/1)
ESD-MM	JEDEC JESD22-A115-A, (200V)	1	3	(0/1)
Latch Up	JEDEC JESD78B Class II (2), 125°C; Level B $\pm 60\text{mA}$	1	6	(0/1)
Mechanical Shock	JEDEC JESD22-B104C, Mil-Std-883H, method 2002.5, Cond. E, 10,000g's, 0.2ms, $\pm X, Y, Z - 6$ directions, 5 times/direction	3	30	(0/1)
Vibration	JEDEC JESD22-B103B, Variable Frequency (random), Cond. B, 5-500Hz, X, Y, Z - 4 times/direction	3	5	(0/1)
Temperature Cycling (TC) <sup>(1)</sup>	JEDEC JESD22-A104D Condition N, [-40°C to +85°C], Soak Mode 2 [5'], 100 cycles	3	77	(0/1)

#### Board Level Tests

TEST	Method/Condition	Lot Quantity	Sample / Lot	Acc / Reject Criteria
Board Mechanical Shock	JEDEC JESD22-B104C, Mil-Std-883H, method 2002.5, Cond. E, 10000g's, 0.2ms, +X, Y, Z - 6 directions, 5 times/direction	1	5	(0/1)
Board Temperature Cycling (TC) <sup>(1)</sup>	JEDEC JESD22-A104D Condition N, [-40°C to +85°C], Soak Mode 2 [5'], 100 cycles	1	40	(0/1)

(1) Tests are preceded by MSL3 Preconditioning in accordance with JEDEC JESD22-A113F



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**9 Environmental Compliance**

The IDG/IXZ-21X0 is RoHS and Green compliant.

The IDG/IXZ-21X0 is in full environmental compliance as evidenced in report HS-IDG/IXZ-21X0, Materials Declaration Data Sheet.

**Environmental Declaration Disclaimer:**

InvenSense believes this environmental information to be correct but cannot guarantee accuracy or completeness. Conformity documents for the above component constitutes are on file. InvenSense subcontracts manufacturing and the information contained herein is based on data received from vendors and suppliers, which has not been validated by InvenSense.

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